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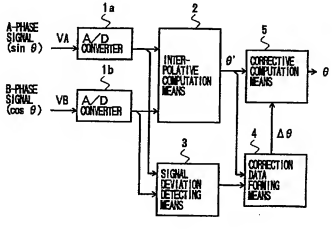
(54) INTERPOLATION CIRCUIT OF ENCODER

(57) An encoder interpolation circuit for obtaining interpolation data within one wave from two sine-wave encoder signals of different phases comprises interpolative computation means (2) for receiving two sine-wave encoder signals received and carrying out to interpolative computation within one wave, signal deviation detecting means (3) for detecting a deviation of the two sine-wave encoder signals, correction data forming means (4) for outputting correction data corresponding to the detected deviation and the output of the interpolative computation means, and corrective computation means (5) for obtaining the corrected interpolation data by carrying out corrective computation for the output of the interpolative computation means with the correction data and obtaining corrected interpolation data.

FIG. 1



EP 0 874 223 A1

Description

TECHNICAL FIELD

The present invention relates to an interpolation circuit for interpolating detection signals from an encoder for detecting rotational angles or positions on a straight line.

BACKGROUND ART

In a detecting device for detecting positions of a table and a motor of a machine tool of an NC apparatus, a rotary-type pulse encoder attached to the motor shaft or the like and a linear-type pulse encoder attached to a worktable or the like are known as means for detecting the movement and moving speed of a moving body. As the moving body moves, these encoders generate an A-phase signal, a sine-wave signal ($K\sin\theta$), and a B-phase sine-wave signal ($K\sin(\theta \pm \pi/2)$), which has a phase difference of 90° from the A-phase signal, and obtains angle data (θ) by carrying out interpolative computation with use of these two sine-wave signals, hereby improving the resolution for the position and speed.

There are known methods for this interpolation technique, including a method in which a converter circuit for sine- and cosine-wave signals from a signal source is composed of a plurality of resistors and comparator arrays. In another method based on the interpolation circuit configuration shown in FIG. 15, a sine-wave signal V_A and a cosine-wave signal V_B are inputted to the interpolative computation means 2 after being A/D-converted by means of A/D converters 1a and 2a, respectively, and the interpolative computation means 2 computes $\tan^{-1}(V_A/V_B)$ to obtain angle data θ. The computation of this inverse transform of a tangent can be carried out by using a calculation process based on Taylor expansion, for example.

An interpolation circuit used for a conventional encoder carries out interpolative computation on the assumption that it receives an A-phase signal (sine-wave signal) and a B-phase signal (cosine-wave signal) that are equal in amplitude K and have a phase difference of $\pi/2$.

In general, however, A- and B-phase signals that are inputted to an encoder do not always have an accurate phase difference of $\pi/2$, and are not always equal in amplitude. In other words, the phase difference between the two signals may be deviated from $\pi/2$ or the amplitude ratio may be deviated from 1.

If interpolative computation is carried out with use of these deviated signals, the obtained angle θ may possibly be subject to an interpolation error attributable to the deviation.

Conventionally, therefore, this interpolation error is removed by a method in which an analog regulator circuit is provided in front of A/D converters so that the amplitude ratio between the A- and B-phase signals inputted to the analog regulator circuit can be adjusted to 1 or that phase difference between the A- and B-phase signals can be adjusted to $\pi/2$. However, the removal of the interpolation error by means of the analog regulator circuit requires a complicated circuit configuration. Since the regulator circuit is an analog circuit, moreover, it is necessary to adjust the regulator circuit itself.

DISCLOSURE OF THE INVENTION

The object of the present invention is to provide an interpolation circuit for and encoder, in which interpolation data cleared of an interpolation error that is attributable to signal deviations can be obtained by correcting interpolation data, which is obtained by interpolative computation, without adjusting input signals.

In order to achieve the above object, an encoder interpolation circuit according to the present invention comprises: interpolative computation means for receiving two encoder signals of difference phases, carrying out interpolative computation for these signals and outputting interpolation angle data, correction data forming means for obtaining and outputting correction data corresponding to a combination of a detected deviation of the two encoder signals from a normal waveform and the interpolation angle data outputted from the interpolative computation means; and corrective computation means for correcting the interpolation angle data outputted from the interpolative computation means with the correction data outputted from the correction data forming means and outputting corrected interpolation angle data.

Preferably, the deviation of the two encoder signals is the ratio of the amplitude of one sine-wave encoder signal to the amplitude of the other sine-wave encoder signal.

Preferably, the deviation of the two encoder signals is a phase error as the difference between the predetermined a phase difference between two encoder signals and an actual phase difference between the two encoder signals.

Preferably, the correction data forming means forms the correction data by substituting an output of the interpolative computation means and a detected phase error, as a deviation of the two encoder signals, individually for variables in a computational expression for obtaining preset correction data and operating the computational expression.

Preferably, the correction data forming means is previously stored with the value of correction data for a combina-

tion of the output of the interpolative computation means and the output of the correction data forming means, and the correction data forming means receives the output of the interpolative computation means and the output of the correction data forming means and outputs the correction data corresponding to the combination of these outputs.

Preferably, the correction data stored in the correction data forming means can be fetched with an address which represents a combination of the output of the interpolative computation means and the output of the correction data forming means.

Further preferably, the correction data forming means is stored with a data table so that corresponding data can be fetched with an address which represents a combination of angle data in a limited range and a detected signal deviation, and the correction data forming means includes means for receiving the detected deviation of the two encoder signals and the output of the interpolative computation means, and determining an address based on the deviation and the output, and means for forming the correction data by accessing said data table to fetch the corresponding data with the determined address and processing the fetched data.

According to the present invention, interpolation data cleared of an interpolation error that is attributable to signal deviations can be obtained by correcting interpolation data, which is obtained by interpolative computation, without adjusting input signals.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram for illustrating an outline of an encoder interpolation circuit according to the present invention;

FIG. 2 is a block diagram for illustrating an encoder interpolation circuit according to a first embodiment of the present invention;

FIG. 3 is a block diagram for illustrating an encoder interpolation circuit according to a second embodiment of the present invention;

FIG. 4 is a diagram for illustrating an amplitude ratio between two encoder signals;

FIG. 5 is a diagram for illustrating an error included in interpolation data when the amplitude difference between the two encoder signals is deviated from $\pi/2$;

FIG. 6 is a diagram schematically showing a pattern of an error included in computed interpolation data as the amplitude ratio between the two encoder signals is deviated from 1;

FIG. 7 is a block diagram for illustrating elements constituting correction data storage means in the encoder interpolation circuit of FIG. 3;

FIG. 8 is a diagram schematically showing correction data patterns for canceling the error shown in FIG. 6, according to the amplitude ratio;

FIG. 9 is a block diagram for illustrating an encoder interpolation circuit according to a third embodiment of the present invention;

FIG. 10 is a block diagram for illustrating an encoder interpolation circuit according to a fourth embodiment of the present invention;

FIG. 11 is a diagram for illustrating phase errors between two encoder signals;

FIG. 12 is a diagram schematically showing a pattern of an error included in computed interpolation data as the phase difference between the two encoder signals is deviated from $\pi/2$;

FIG. 13 is a block diagram for illustrating elements constituting correction data storage means in the encoder interpolation circuit of FIG. 10;

FIG. 14 is a diagram schematically showing correction data patterns for canceling the error shown in FIG. 12 according to the error attributable to the phase difference; and

FIG. 15 is a diagram for illustrating a conventional encoder interpolation circuit.

BEST MODE FOR CARRYING OUT THE INVENTION

[Outline of Encoder Interpolation Circuit]

Referring first to the block diagram of FIG. 1, an outline of an interpolation circuit for an encoder according to the present invention will be described.

One encoder signal (A-phase signal; sine-wave signal) V_A and another encoder signal (B-phase signal; cosine-wave signal) V_B having the same amplitude as and a phase difference of 90 degrees from V_A are converted from analog signals into digital signals by means of A/D converters 1a and 1b, respectively. The A-phase signal V_A and the B-phase signal V_B, converted into the digital signals by the A/D converters 1a and 1b, are inputted to the interpolative computation means 2. The interpolative computation means 2 computes

$$\theta' = \tan^{-1}(V_A/V_B),$$

and outputs interpolation data θ '. The interpolation data θ ' includes an error (interpolation error δ θ) that depends on a deviation in amplitude between the A-phase signal V_A and the B-phase signal V_B or a deviation in phase difference.

The A-phase signal V_A and the B-phase signal V_B, converted into the digital signals by the A/D converters 1a and 1b, are also inputted to the signal deviation detecting means 3, whereupon deviations (differences in amplitude or phase) between the A-phase signal V_A and the B-phase signal V_B are detected.

Correction data forming means 4 receives the output (interpolation data θ ') of the interpolative computation means 2 and the output of the signal deviation detecting means 3, and obtains correction data Δ θ from these data.

Receiving the output θ ' of the interpolative computation means 2 and the output Δ θ of the correction data forming means 4, corrective computation means 5 calculates

$$\theta = \theta' + \Delta\theta,$$

and outputs interpolation data θ that includes no interpolation error.

[Case in which the signal deviation between the A- and B-phase signals V_A and V_B is detected by the amplitude difference between the two signals]

Referring now to FIGS. 2 to 8, there will be described a case in which a signal deviation to be detected by the signal deviation detecting means 3 of FIG. 1 is the amplitude difference between the A-phase signal V_A and the B-phase signal V_B, specifically.

(First Embodiment)

Referring now to the block diagram of FIG. 2, there is explained a first embodiment of the encoder interpolation circuit for this case. The encoder interpolation circuit shown in the block diagram of FIG. 2 has the same configuration as the encoder interpolation circuit shown in the block diagram of FIG. 1, except that, in this embodiment, the signal deviation detecting means 3 of the encoder interpolation circuit shown in the block diagram of FIG. 1 is replaced with the amplitude ratio detecting means 3k. Accordingly, description of other components than the amplitude ratio detecting means 3k in the encoder interpolation circuit of FIG. 2 will be omitted. The interpolative computation means 2 receives the respective outputs of the A/D converters 1a and 1b, that is, the A-phase signal V_A and the B-phase signal V_B converted into the digital signals, and executes interpolative computation within one wave (section from 0 to 2π).

Referring now to FIG. 4, an amplitude ratio k between the two encoder signals V_A and V_B will be described. For simplicity of illustration in FIG. 4, the encoder signal V_A as a sine-wave signal and the B-phase signal V_B as a cosine-wave signal are represented by a triangular wave each. It is supposed that there is an exact phase difference of π/2 between these two encoder signals V_A and V_B. However, it is supposed that the two signals V_A and V_B are not equal in amplitude.

Referring to FIG. 4, if the values of the encoder signals V_A at a zero-cross time point for the encoder signal V_B are V_{AH} and V_{AL}, and if the values of the encoder signals V_B at zero-cross time points for the encoder signal V_A are V_{BH} and V_{BL}, the amplitude ratio k is given by the following expressions.

If $(V_{AH}-V_{AL})>(V_{BH}-V_{BL})$ is given, we obtain

$C_{AB} = 0$,

$$k = (V_{AH}-V_{AL})/(V_{BH}-V_{BL}). \quad (1)$$

If $(V_{AH}-V_{AL}) < (V_{BH}-V_{BL})$ is given, we obtain

$C_{AB} = 1$,

$$k = (V_{BH}-V_{BL})/(V_{AH}-V_{AL}). \quad (2)$$

In the above equations, C_{AB} is a comparison flag that indicates the result of comparison between the respective amplitudes of the encoder signals V_A and V_B. $C_{AB} = 0$ represents the case where the amplitude of the signal V_A is greater than the amplitude of the signal V_B, while $C_{AB} = 1$ represents the case where the amplitude of the signal V_A is smaller than the amplitude of the signal V_B.

The amplitude ratio data k and the state of the flag C_{AB} can be obtained by monitoring the values of the A/D converters 1a and 1b, sampling one of the values at a time when the other of the values turns to be zero and calculating a

mean value of the sampled data.

If the amplitude ratio k between the two encoder signals V_A and V_B is 1, each of these two signals V_A and V_B is represented by one point on a circle that is described around the origin of a rectangular coordinate system, as shown in FIG. 5. Thus, the value for the axis of abscissa corresponding to the one point on the circle is V_B, the value for the axis of ordinate is V_A, and the angle of a straight line that connects this point and the origin is given as angle data θ. If the amplitude of the encoder signal V_A is greater than the amplitude of the encoder signal V_B so that k is not at 1, each of these signals V_A and V_B is represented by one point on an ellipse, not a circle. If the amplitude of the signal V_A is greater than the amplitude of the signal V_B, as shown in FIG. 5, when the one of the encoder signals is V_B, for example, the other of the encoder signals is kV_A(k>1), not V_A. The angle of a straight line that connects the one point (V_B, kV_A) on the ellipse and the origin is given as the interpolation data θ '. Inevitably, therefore, the interpolation data θ ' is computed in accordance with the signals kV_A and V_B. As shown in FIG. 5, the interpolation data θ ' includes an error (interpolation error), $\delta\theta$ (= θ ' — θ).

If there is exact phase difference of $\pi/2$ between the two of the encoder signals V_A and V_B, that is, if the one and the other of the encoder signals V_A and V_B are sine- and cosine-wave signals, respectively, the interpolation data θ shown in FIG. 5 and the interpolation error $\delta\theta$ have the relation shown in FIG. 6, for example. Referring to FIG. 6, a pattern of $\delta\theta$ within the range of θ = 0 to $\pi/2$ is the same as a pattern of $\delta\theta$ within the range of $\theta = \pi$ to $3\pi/2$. Further, a pattern of $\delta\theta$ within the range of $\theta = \pi/2$ to π is the same as a pattern of $\delta\theta$ within the range of $\theta = 3\pi/2\pi$ to 2π. Furthermore, the pattern of $\delta\theta$ within the range of $\theta = \pi/2$ to π and the pattern of $\delta\theta$ within the range of θ = 0 to $\pi/2$ are in point symmetry with respect to a point $\theta = \pi/2$.

The following is a description of the correction data $\Delta\theta$ for the interpolation data θ ' that includes the interpolation error in the case where amplitude ratio between the sine-wave encoder signal (A-phase signal) and the cosine-wave encoder signal (B-phase signal) is at k ($\neq$ 1).

Using the A-phase signal (hereinafter designated by kV_A) and the B-phase signal (hereinafter designated by V_B), the interpolation data θ ' that includes the interpolation error is given by

$$\theta' = \tan^{-1}(kV_A/V_B), \tag{3}$$

From the above expression (3), the following expressions are obtained.

$$kV_A/V_B = \sin\theta'/\cos\theta', \tag{4}$$

$$V_A/V_B = \sin\theta'/k\cos\theta'. \tag{5}$$

On the other hand, the interpolation data θ that includes no interpolation error with k = 1 is given by

$$\theta = \tan^{-1}(V_A/V_B), \tag{6}$$

Accordingly, the correction data $\Delta\theta$ can be represented as follows:

$$\Delta\theta = \theta - \theta' = \tan^{-1}(\sin\theta'/k\cos\theta') - \theta' \tag{7}$$

The above expression (7) indicates that the correction data $\Delta\theta$ can be obtained from the interpolation data θ ' that includes the interpolation error and the amplitude ratio k.

Based on the interpolation data θ ' received from the interpolative computation means 2 and the amplitude ratio k received from the amplitude ratio detecting means 3k, therefore, correction data computation means 4k1 of FIG. 2 carries out computation according to the aforesaid expression (7), and obtains and outputs the correction data $\Delta\theta$.

Based on the interpolation data θ ' received from the interpolative computation means 2 and the correction data $\Delta\theta$ received from correction data storage means 4k1, therefore, the corrective computation means 5 calculates

$$\theta = \theta' + \Delta\theta, \tag{8}$$

and outputs the interpolation data θ obtained by correcting the interpolation error $\delta\theta$.

(Second Embodiment)

In the first embodiment shown in FIG. 2, the correction data $\Delta\theta$ is obtained by the computation of expression (7) by means of the correction data computation means 4k1. Instead of obtaining the correction data $\Delta\theta$ by this computation, however, the correction data $\Delta\theta$ corresponding to a combination of the input value θ ' and k may be read out after

previously storing the correction data storage means with the relation between the input value (θ ', k) and the correction data Δ θ corresponding to this input value in the form of a table.

Referring now to the block diagram of FIG. 3, there is shown an encoder interpolation circuit according to a second embodiment, which is provided with the aforesaid correction data storage means in place of the correction data computation means 4k1.

The encoder interpolation circuit shown in the block diagram of FIG. 3 has the same configuration as the encoder interpolation circuit shown in the block diagram of FIG. 2, except that, in this embodiment, the correction data computation means 4k1 of the encoder interpolation circuit shown in the block diagram of FIG. 2 is replaced with correction data storage means 4k2. Accordingly, description of other components than the correction data computation means 4k1 in the encoder interpolation circuit shown in the block diagram of FIG. 3 will be omitted.

The correction data storage means 4k2 is stored with correction data Δ θ corresponding to combinations (k, θ ') of various amplitude ratios k and the interpolation data θ '. The correction data storage means 4k2 receives the amplitude ratios k and the interpolation data θ ' from the interpolative computation means 2 and amplitude ratio detecting means 3k1, and reads out the correction data Δ θ according to the address (k, θ ').

A large storage capacity is needed to load the correction data storage means 4k2 with the correction data to cope with all the possible combinations of the amplitude ratios k and the interpolation data θ '. However, there is a method in which correction data can be fetched for all the possible combinations of the amplitude ratios k and the interpolation data θ ' even if the range of the interpolation data θ ' and the amplitude ratios k are limited to reduce the quantity of data to be stored in the correction data storage means 4k2 correspondingly. The following is a description of this method.

As mentioned before with reference to FIGS. 5 and 6, from the pattern of the interpolation error δ θ within the range of the interpolation data θ = 0 to π/2 (first quadrant), the pattern of the interpolation error δ θ within the range of the interpolation data θ = π/2 to π (second quadrant), the pattern of the interpolation error δ θ within the range of the interpolation data θ = π to 3π/2 (third quadrant), and the pattern of the interpolation error δ θ within the range of the interpolation data θ = 3π/2 to 2π (fourth quadrant) can be obtained individually. Therefore, regarding the correction data Δ θ for canceling the interpolation error δ θ, it is sufficient to store only the pattern of the correction data Δ θ within the range of the interpolation data θ ' (output of the interpolative computation means 2) = 0 to π/2 (first quadrant). The quantity of data stored in the correction data storage means 4 can be reduced by the storage of the correction data within this limited range.

If the value of the interpolation error δ θ is small, the value of the interpolation error δ θ and the amplitude ratio k can be considered to be substantially in proportion to each other. Accordingly, only correction data Δ θ 0 for a specific amplitude ratio k0 is stored in advance so that correction data Δ θ n for other amplitude ratios kn can be obtained by multiplying the correction data for the specific amplitude ratio k0 by the percentage of the amplitude ratio. Thus, the number of amplitude ratios k to be stored in the correction data storage means 4k2 can be limited to reduce the quantity of correction data stored.

The block diagram of FIG. 7 illustrates the configuration of the correction data storage means 4k2 for limiting the range of the interpolation data θ ' and the amplitude ratios k and storing the correction data. The correction data storage means 4k2 comprises an address converter circuit 11, correction data table 12, sign inversion selector circuit 13, and multiplier circuit 14. The address converter circuit 11 receives the interpolation data θ ' and the comparison flag C_{AB} and forms addresses. The correction data table 12 is loaded only with the correction data corresponding to combinations of the interpolation data θ ' in the limited range and the limited amplitude ratios k, and the correction data are read out from the table 12 in response to address assignment by means of the address converter circuit 11. The sign inversion selector circuit 13 inverts the sign of the read correction data in accordance with the computed interpolation data θ ' and the comparison flag C_{AB}. The multiplier circuit 14 multiplies the correction data by the detected amplitude ratio k.

FIG. 8 shows the relation between the correction data Δ θ and the interpolation data θ ' represented for each amplitude ratio k. Referring to FIG. 8, each correction data Δ θ has a size and sign which cancel the interpolation error δ θ based on the amplitude ratio k shown in FIG. 6. A pattern of Δ θ within the range of the interpolation data θ ' = 0 to π/2 is the same as a pattern of Δ θ within the range of θ ' = π to 3π/2. Further, a pattern of Δ θ within the range of θ ' = π/2 to π is the same as a pattern of Δ θ within the range of θ ' = 3π/2π to 2π . Furthermore, the pattern of Δ θ within the range of θ ' = π/2 to π and the pattern of Δ θ within the range of θ ' = 0 to π/2 are symmetrical with respect to a point θ = π/2. Accordingly, only the patterns of Δ θ within the range of θ ' = 0 to π/2 are stored, and the correction data within the range of the correction data θ ' = π/2 to 2π can be obtained from the patterns of Δ θ within the range of the interpolation data θ ' = 0 to π/2 .

Further, the correction data Δ θ , which changes its size depending on the amplitude ratio k, can be considered to be substantially proportional to the percentage of the amplitude ratio k when the amplitude ratio k is low. The correction data Δ θ is stored as a representative value for the specific amplitude ratio k, and the other amplitude ratios k can be obtained by multiplication.

FIG. 8 illustratively shows cases for k = 1.0, k = 1.02, k = 1.04, and k = 1.06. For example, only the correction data Δ θ for k = 1.02 is stored, and the other amplitude ratios k can be obtained by multiplying the correction data Δ θ by the ratio to k = 1.02 as a multiplication factor. Here k = 1.0 indicates that the respective amplitudes of the two encoder sig-

nals are equal.

The address converter circuit 11 is a circuit that receives the computed interpolation data θ ' and the comparison flag C_{AB}, and forms addresses for reading out the correction data table 12. In forming the addresses, the addresses are outputted depending on the range of the inputted interpolation data θ ' and the sign, positive or negative, of the comparison flag C_{AB}, with $0 \leqq \theta' < \pi/2$ as a unit, as shown in Table 1 below.

The sign inversion selector circuit 13 does or does not invert the sign of the data read out from the correction data table 12, depending on the range of the computed interpolation data θ ' and the sign, positive or negative, of the comparison flag C_{AB}, as shown in Table 1.

【Table 1】

θ '	Comparison Flag C_{AB}	Address to Data Table	Sign of Output Data
$0 \leqq \theta' < \pi/2$	0 (A>B)	θ'	Non-inverted
	1 (A<B)	$\pi/2 - \theta'$	Inverted
$\pi/2 \leqq \theta' < 0$	0 (A>B)	$\pi - \theta'$	Inverted
	1 (A<B)	$\theta' - \pi/2$	Non-inverted
$\pi \leqq \theta' < 3\pi/2$	0 (A>B)	$\theta' - \pi$	Non-inverted
	1 (A<B)	$3\pi/2 - \theta'$	Inverted
$3\pi/2 \leqq \theta' < 2\pi$	0 (A>B)	$2\pi - \theta'$	Inverted
	1 (A<B)	$\theta' - 3\pi/2$	Non-inverted

Further, the multiplier circuit 14 is a circuit that multiplies the correction data stored for the specific amplitude ratio k by a multiplication factor of a percentage corresponding to the current amplitude ratio k. Table 2 below shows examples of the multiplication factor. The correction data is stored in advance as a reference for the amplitude ratio k = 1.02, and different amplitude ratios k are obtained by multiplication by specific multiplication factors on the basis of the amplitude ratio k = 1.02 as a reference.

【Table 2】

Amplitude Ratio K	Multiplication Factor
$1.00 \leqq k < 1.01$	0
$1.01 \leqq k < 1.03$	1
$1.03 \leqq k < 1.05$	2
$1.05 \leqq k < 1.07$	3
$1.07 \leqq k$	4

In the case where the amplitude ratio k ranges from 1.03 to 1.05, for example, the correction data for the amplitude ratio k = 1.02 is multiplied by a multiplication factor of 2. In the case where the amplitude ratio k ranges from 1.05 to 1.07, the correction data Δ θ is obtained by multiplying the correction data for the amplitude ratio k = 1.02 by a multiplication factor of 3.

In a method of multiplication in the multiplier circuit 14, moreover, the correction data Δ θ may be obtained by determining the multiplication factor in a manner such that the correction data table 12 is stored with only correction data for a specific amplitude ratio k1 in the case where the amplitude of the one encoder signal is greater than the amplitude of the other encoder signal, and the correction data is multiplied by (1 - k)/(1 — k1) when the detected amplitude ratio k is higher than 1 or multiplied by -(1 - k)/(1 — k1) when the detected amplitude ratio k is lower than 1.

In a method of multiplication in the multiplier circuit 14, furthermore, the correction data $\Delta\theta$ may be obtained by determining the multiplication factor in a manner such that the correction data table 12 is stored with first correction data for a specific amplitude ratio k1 in the case where the amplitude of the one encoder signal is greater than the amplitude of the other encoder signal, and second correction data for a specific amplitude ratio k2 in the case where the amplitude of the one encoder signal is smaller than the amplitude of the other encoder signal, and the first correction data is multiplied by (1 - k)/(1 — k1) when the detected amplitude ratio k is higher than 1, while the second correction data is multiplied by (1 - k)/(1 — k2) when the detected amplitude ratio k is lower than 1.

[Case in which the signal deviation between the A- and B-phase signals V_A and V_B is detected by the phase difference between the two signals]

Referring now to FIGS. 9 to 14, there will be described an encoder interpolation circuit for correcting an interpolation error based on the phase error between the two encoder signals.

(First Embodiment)

Referring to the block diagram of FIG. 9, there is shown a first embodiment of the encoder interpolation circuit for this case. The encoder interpolation circuit shown in the block diagram of FIG. 9 has the same configuration as the encoder interpolation circuit shown in the block diagram of FIG. 1, except that, in this embodiment, the signal deviation detecting means 3 of the encoder interpolation circuit shown in the block diagram of FIG. 1 is replaced with phase error detecting means 3p. Accordingly, a description of other components than the phase error detecting means 3p of the encoder interpolation circuit shown in the block diagram of FIG. 9 will be omitted.

Referring now to FIG. 11, the phase error between the two encoder signals will be described. In FIG. 11, the sine- and cosine-wave signals are simplified in the form of triangular waves and are designated by V_A and V_B, respectively. Although these two encoder signals V_A and V_B are equal in amplitude, it is supposed that their phase difference is deviated from $\pi/2$ (that is, a phase error exists).

For detecting a phase error Pd between these two encoder signals V_A and V_B, a zero-cross point for the encoder signal V_A is selected as a starting point and then the times t1, t2, t3, t4 and t5 at the zero-cross points for the signals are measured. Thereupon, the phase error Pd can be obtained as follows:

$$\text{Phase difference } P1 = \{(t1 + t3)/2 - t2/2)\}/t4 \times 2\pi, \tag{9}$$

$$\text{Phase difference } P2 = \{(t3 + t5)/2 - (t2/2 + t4/2)\}/t4 \times 2\pi, \tag{10}$$

$$\text{Phase difference } P = (P1 + P2)/2, \tag{11}$$

$$\text{Phase error } Pd = P - t4/4 \times 2\pi. \tag{12}$$

Although the average of the phase differences P1 and P2 is obtained according to the above expression in order to improve the detection accuracy, the phase error may be also obtained from the phase difference P1 only.

In obtaining the foregoing phase error Pd, measurement has to be is made in a state such that the moving speed of an object to be detected is so stable that variation in the speed during the time from t1 to t5 is negligible. Further, the phase error is obtained by calculating a mean value after sampling data during a plurality of cycles of input signals.

If the two encoder signals V_A and V_B are deviated from the phase difference of $\pi/2$ (i.e., if an error in the phase difference is produced), the error $\delta\theta$ included in the interpolation data θ' computed based on the signals V_A and V_B has a pattern such as the one shown in the diagram of FIG. 12. FIG. 12 schematically shows the relation between the error $\delta\theta$ and real angle data θ that does not include the error $\delta\theta$. A pattern of the error $\delta\theta$ within the range of the angle data $\theta = 0$ to π and a pattern of the error $\delta\theta$ within the range of the angle data $\theta = \pi$ to 2π are bisymmetrical with respect to a point $\theta = \pi$.

It is supposed that the phase difference between the two encoder signals is deviated from $\pi/2$ by Pd, so that the interpolation data θ', deviated from the real value θ by $\Delta\theta$, is given when an interpolative computation is carried out for these encoder signals. In order to cancel the interpolation error $\delta\theta$, therefore, the correction data $\Delta\theta$ is given to the interpolation data θ'.

In this case, the following expression is established among the interpolation data θ' that includes the interpolation error $\delta\theta$, real angle θ, and phase error Pd:

$$\theta' = \tan^{-1}(\sin\theta / \cos(\theta - Pd)). \tag{13}$$

Accordingly, we obtain

$$\sin\theta'/\cos\theta' = \sin\theta/\cos\theta\,(\theta - Pd) = \sin\theta/\{\cos\theta \cdot \cos(Pd) + \sin\theta \cdot \sin(Pd)\}. \quad (14)$$

From expression (14), we obtain

$$\sin\theta/\cos\theta = \sin\theta' \cdot \cos(Pd)/(\cos\theta' - \sin\theta' \cdot \sin(Pd)). \quad (15)$$

Accordingly, the real angle θ is given by the following expression:

$$\theta = \tan^{-1}\{(\sin\theta' \cdot \cos(Pd)/(\cos\theta' - \sin\theta' \cdot \sin(Pd))\}. \quad (16)$$

Based on the above expression (16), the correction data Δθ is given by the following expression:

$$\Delta\theta = \theta - \theta' = \tan^{-1}\{(\sin\theta' \cdot \cos(Pd)/(\cos\theta' - \sin\theta' \cdot \sin(Pd))\} - \theta'. \quad (17)$$

The above expression (17) indicates that the correction data Δθ can be obtained from the phase error Pd and the interpolation data θ' that includes the interpolation error δθ.

Thereupon, correction data computation means 4p1 of FIG. 9 carries out computation based on the aforesaid expression (17) in accordance with the interpolation data θ' received from the interpolative computation means 2 and the phase error Pd received from the phase error detecting means 3p, and obtains and outputs the correction data Δθ.

Based on the interpolation data θ' received from the interpolative computation means 2 and the correction data Δθ received from the correction data computation means 4p1, therefore, the corrective computation means 5 of FIG. 9 calculates

$$\theta = \theta' + \Delta\theta, \quad (18)$$

and outputs the real angle, that is, the interpolation data θ, obtained after the correction of the interpolation error δθ.

(Second Embodiment)

In the first embodiment shown in FIG. 9, the correction data Δθ is obtained by the computation of expression (17) by means of the correction data computation means 4p1. Correction data storage means 4p2 may be used in place of the correction data computation means 4p1 for this computation. An encoder interpolation circuit according to this second embodiment is shown in the block diagram of FIG. 10.

The encoder interpolation circuit shown in the block diagram of FIG. 10 has the same configuration as the encoder interpolation circuit shown in the block diagram of FIG. 9, except that, in this embodiment, the correction data computation means 4p1 of the encoder interpolation circuit shown in the block diagram of FIG. 9 is replaced with the correction data storage means 4p2. Accordingly, a description of other components than the correction data storage means 4p2 in the encoder interpolation circuit of FIG. 10 will be omitted.

The correction data storage means 4p2 is stored with correction data Δθ corresponding to combinations (Pd, θ') of various phase errors Pd and the interpolation data θ'. The correction data storage means 4p2 receives the phase errors Pd and the interpolation data θ' from the interpolative computation means 2 and the phase error detecting means 3p, and reads out the correction data Δθ according to the address (Pd, θ').

A large storage capacity is required for loading the correction data Δθ so as to cope with all the possible combinations of the phase errors Pd and the interpolation data θ'. There is a method in which the correction data can be fetched for all the possible combinations of the phase errors Pd and the interpolation data θ' even if the range of the interpolation data θ' and the phase errors Pd are limited to reduce the quantity of data to be stored in the correction data storage means 4p2 correspondingly. The following is a description of this method.

As shown in FIG. 12, the pattern of the interpolation error δθ within the range of the angle data θ = 0 to π and the pattern of the interpolation error δθ within the range the angle data θ = π to 2π are symmetrical with respect to θ = π. Accordingly, regarding the correction data Δθ for canceling the interpolation error δθ included in the interpolation data θ', it is sufficient to store in the correction data storage means 4p2 only the correction data Δθ within the range of the interpolation data θ' = 0 to π. Within the range of the interpolation data θ' = π to 2π, corresponding correction data Δθ can be obtained by utilizing the symmetry with the data stored in the correction data storage means 4p2. The quantity of stored correction data can be reduced by limiting the range of the interpolation data θ' to be stored.

If the error amount of the interpolation error is small, the error amount and the phase errors Pd can be considered to be substantially in proportion to one another. Accordingly, only correction data for a specific phase error Pd is stored

in advance so that correction data for other phase errors Pd can be obtained by multiplying the correction data for the specific phase error Pd0 by the percentage of the phase errors. Thus, the phase errors Pd can be limited to reduce the quantity of correction data stored.

The block diagram of FIG. 13 illustrates the configuration of the correction data storage means 4p2 for storing the correction data by limiting the range of the interpolation data θ' and the phase errors Pd. In FIG. 13, the correction data storage means 4p2 comprises an address converter circuit 21, correction data table 22, sign inversion selector circuit 23, and multiplier circuit 24. The address converter circuit 21 receives the interpolation data θ' and the phase errors Pd and forms addresses. The correction data table 22 is loaded only with the correction data corresponding to combinations of the interpolation data θ' in the limited range and the limited phase errors Pd, and the correction data are read out from the table 22 in response to address assignment by means of the address converter circuit 21. The sign inversion selector circuit 23 inverts the sign of the read correction data in accordance with the phase errors Pd. The multiplier circuit 24 multiplies the correction data by the phase errors Pd.

FIG. 14 is a diagram showing relations between correction data $\Delta\theta$ for the interpolation error based on the phase errors Pd and the interpolation data θ'. Referring to FIG. 14, each correction data $\Delta\theta$ has a size and sign such as to cancel the interpolation error $\delta\theta$ shown in FIG. 12. Since, the correction data $\Delta\theta$ within the range of $\theta = 0$ to π is symmetrical with the correction data $\Delta\theta$ within the range of $\theta = \pi$ to 2π, the correction data $\Delta\theta$ within the range of $\theta = \pi$ to 2π can be obtained from the stored corrected data within the range of $\theta = 0$ to π.

Further, the correction data $\Delta\theta$, which changes its size depending on the phase errors Pd, can be considered to be substantially proportional to the percentage of the phase errors Pd when the phase errors Pd are small. The correction data $\Delta\theta$ is stored as a representative value for a specific phase error Pd, and the other phase errors Pd can be obtained by multiplication. FIG. 14 illustratively shows cases for Pd = 1.0°, Pd = 2.0°, and Pd = 3.0°. For example, only the correction data $\Delta\theta$ for Pd = 1.0° is stored, and the correction data for the other phase errors Pd can be obtained by multiplying the correction data $\Delta\theta$ by the ratio to Pd = 1.0° as a multiplication factor. Here Pd = 0° indicates that there is no phase error between the two encoder signals.

The address converter circuit 21 is a circuit that receives the computed interpolation data θ' and the detected phase errors Pd, and forms addresses for reading out the correction data table 22. In forming the addresses, the addresses are outputted depending on the range of θ' and the sign, positive or negative, of the phase errors Pd, with $0 \leq \theta' < \pi$ as a unit, as shown in Table 3 below.

Further, the sign inversion selector circuit 23 does or does not invert the sign of the data read out from the correction data table 22, depending on the range of the computed interpolation data θ' and the sign, positive or negative, of the phase errors Pd, as shown in Table 3.

【Table 3】

θ'	Sign of Pd	Address to Data Table	Sign of Output Data
$0 \leqq \theta' < \pi$	Positive	θ'	Non-inverted
	Negative	$\pi - \theta'$	Inverted
$\pi \leqq \theta' < 2\pi$	Positive	$\theta' - \pi$	Non-inverted
	Negative	$2\pi - \theta'$	Inverted

Further, the multiplier circuit 24 is a circuit that multiplies the correction data stored for the specific phase error Pd by a multiplication factor of a percentage corresponding to a phase error Pd. Table 4 below shows examples of the multiplication factors. The correction data is stored in advance as a reference for the phase error Pd = 1.0°, and correction data for different phase errors Pd are obtained by multiplication by a specific multiplication factor which is determined with reference to the multiplication factor for the phase error Pd = 1.0°.

【Table 4】

|Pd|	Coefficient of Multiplication
$0^\circ \leqq \|Pd\| < 0.5^\circ$	0
$0.5^\circ \leqq \|Pd\| < 1.5^\circ$	1
$1.5^\circ \leqq \|Pd\| < 2.5^\circ$	2
$2.5^\circ \leqq \|Pd\| < 3.5^\circ$	3
$3.5^\circ \leqq \|Pd\|$	4

In the case where the phase error Pd ranges from 1.5° to 2.5° , for example, the correction data for the phase error Pd = 1.0° is multiplied by a multiplication factor of 2. In the case where the phase error Pd ranges from 2.5° to 3.5° , the correction data Δ θ is obtained by multiplying the correction data for the phase error Pd = 1.0° by a multiplication factor of 3.

In a method of multiplication in the multiplier circuit 24, moreover, the correction data Δ θ may be obtained by storing the correction data table 22 with only correction data for a specific phase error, and multiplying the read correction data by a factor that is determined by the ratio of the specific phase error to the detected phase error in the case where the specific error and the detected phase error have the same sign or multiplying the read correction data by a factor that is determined by the ratio of the specific phase error to the detected phase error and inverting the sign of the product in the case where the specific error and the detected phase error have different signs.

In a method of multiplication in the multiplier circuit 24, furthermore, the correction data Δ θ may be obtained by storing the correction data table 22 with first correction data for a positive specific phase error and second correction data for a negative specific phase error, multiplying the correction data read out from the first correction data by a factor determined by the ratio of the positive specific phase error to the detected phase error when the detected phase error is positive or multiplying the correction data read out from the second correction data by a factor determined by the ratio of the negative specific phase error to the detected phase error when the detected phase error is negative.

In the embodiment described above, the signal deviation detecting means (amplitude ratio detecting means or phase error detecting means) is incorporated in the encoder interpolation circuit. Alternatively, however, the signal deviation detecting means may be provided outside the encoder interpolation circuit. For example, deviations from a normal waveform may be detected by fetching encoder signals by means of external synchronization or the like. The result of this detection is applied to the input of the correction data forming means.

According to the present invention, as described above, the interpolation error attributable to the amplitude difference and the interpolation error attributable to the phase error can be reduced during the generation of interpolation data.

Claims

1. An encoder interpolation circuit comprising:

interpolative computation means for receiving two encoder signals of difference phases, carrying out interpolative computation for these signals and outputting interpolation angle data;
correction data forming means for obtaining and outputting correction data corresponding to a combination of a detected deviation of the two encoder signals from a normal waveform and the interpolation angle data outputted from said interpolative computation means; and
corrective computation means for correcting the interpolation angle data outputted from said interpolative computation means with the correction data outputted from said correction data forming means and outputting corrected interpolation angle data.

2. An encoder interpolation circuit according to claim 1, wherein said correction data forming means forms the correction data by substituting the output of said interpolative computation means and said detected deviation of the two encoder signals individually for variables in a computational expression for obtaining predetermined correction data and operating the communicational expression.

3. An encoder interpolation circuit according to claim 1, wherein said correction data forming means is previously stored with the value of correction data for a combination of the output of said interpolative computation means and the output of said correction data forming means, and said correction data forming means receives the output of the interpolative computation means and the output of the correction data forming means and outputs the correction data corresponding to the combination of these outputs.

4. An encoder interpolation circuit according to claim 3, wherein said correction data stored in said correction data forming means can be fetched with an address which represents a combination of the output of said interpolative computation means and the output of said correction data forming means.

5. An encoder interpolation circuit according to claim 3, wherein said correction data forming means is stored with a data table so that corresponding data can be fetched with an address which represents a combination of angle data in a limited range and a detected signal deviation, and said correction data forming means includes means for receiving the detected deviation of the two encoder signals and the output of the interpolative computation means, and determining an address based on the deviation and the output, and means for forming said correction data by accessing said data table to fetch the corresponding data with the determined address and processing the fetched data.

6. An encoder interpolation circuit according to claim 3, wherein said correction data forming means is stored with correction data corresponding to a reference signal deviation value and angle data in a limited range, and said correction data forming means includes means for forming said correction data by receiving the detected deviation of the two encoder signals and output of the interpolative computation means, fetching corresponding data from said stored correction data based on the output and the deviation, and carrying out processing including processing in accordance with of the relation between said reference signal deviation value and said detected signal deviation.

7. An encoder interpolation circuit according to claim 1, wherein said deviation of the two encoder signals is the ratio of the amplitude of one sine-wave encoder signal to the amplitude of the other sine-wave encoder signal.

8. An encoder interpolation circuit according to claim 7, wherein said correction data forming means forms the correction data by substituting an output of said interpolative computation means and a detected amplitude ratio, as a detected deviation of the two encoder signals individually for variables in a predetermined computational expression for obtaining correction data and operating the communicational expression.

9. An encoder interpolation circuit according to claim 7, wherein said correction data forming means is stored with data in a table form capable of being fetched with an address representing a combination of the amplitude ratio and the angle data, and said correction data forming means determines said address based on the received deviation of the two encoder signals and the output of the interpolative computation means, fetches data from said table according to the determined address, and outputs the correction data based on the fetched data.

10. An encoder interpolation circuit according to claim 9, wherein said angle data constituting said address ranges from 0 to $\pi/2$.

11. An encoder interpolation circuit according to claim 9, wherein said correction data forming means stores first correction data for a specific amplitude ratio k1 in the case where the amplitude of one encoder signal is greater than the amplitude of the other encoder signal and second correction data for a specific amplitude ratio k2 in the case where the amplitude of the one encoder signal is smaller than the amplitude of the other encoder signal, and multiplies the first correction data by (1 - k)/(1 — k1) when the detected amplitude ratio k is higher than 1 or multiplies the second correction data by (1 - k)/(1 — k2) when the detected amplitude ratio k is lower than 1.

13. An encoder interpolation circuit according to claim 9, wherein said correction data forming means stores only correction data for a specific amplitude ratio k1 in the case where the amplitude of one encoder signal is greater than the amplitude of the other encoder signal, and multiplies the first correction data by (1 - k)/(1 — k1) when the detected amplitude ratio k is higher than 1 or multiplies the correction data by -(1 - k)/(1 — k1) when the detected amplitude ratio k is lower than 1.

14. An encoder interpolation circuit according to claim 1, wherein said deviation ofthe two encoder signals is a phase error as the difference between the predetermined phase difference between two encoder signals and an actual phase difference between the two encoder signals.

15. An encoder interpolation circuit according to claim 14, wherein said correction data forming means forms the correction data by substituting an output of said interpolative computation means and a detected phase error, as a deviation of the two encoder signals, individually for variables in a computational expression for obtaining preset correction data and operating the computational expression.

16. An encoder interpolation circuit according to claim 14, wherein said correction data forming means is stored with data in a table form capable of being fetched with an address representing a combination of said phase error and the angle data, and said correction data forming means determines said address based on the received phase error, as the deviation of the two encoder signals, and output of the interpolative computation means, fetches data from said table according to the determined address, and outputs the correction data based on the fetched data.

17. An encoder interpolation circuit according to claim 16, wherein said predetermined phase difference between two encoder signals is $\pi/2$, and said angle data constituting said address ranges from 0 to π.

18. An encoder interpolation circuit according to claim 16, wherein said correction data forming means stores first correction data for a positive specific phase error and second correction data for a negative specific phase error, and multiplies the first correction data by a factor determined by the positive specific phase error and the detected phase error in the case where the detected phase error is positive or multiplies the second correction data by a factor determined by the negative specific phase error and the detected phase error in the case where the detected phase error is negative.

19. An encoder interpolation circuit according to claim 16, wherein said correction data forming means stores only correction data for a specific phase error, and multiplies the read correction data by a factor determined by the specific phase error and the detected phase error in the case where the specific error and the detected phase error have the same sign or multiplies the read correction data by a factor determined by the specific phase error and the detected phase error in the case where the specific error and the detected phase error have different signs and inverts the sign.

FIG. 1

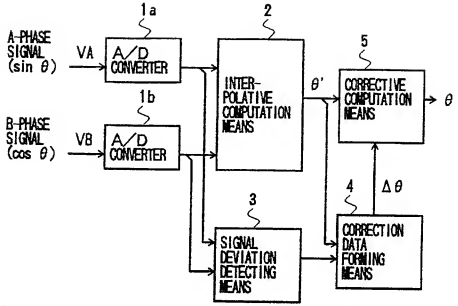
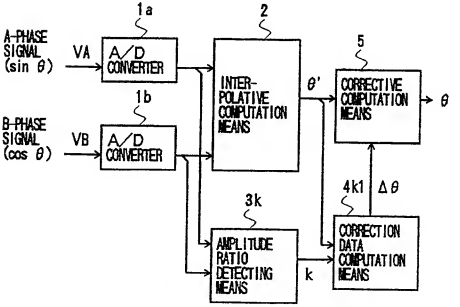

1a
2
A-PHASE SIGNAL (sin θ)
VA
A/D CONVERTER
1b
B-PHASE SIGNAL (cos θ)
VB
A/D CONVERTER
INTER-POLATIVE COMPUTATION MEANS
θ'
5
CORRECTIVE COMPUTATION MEANS
θ
4
Δθ
3
SIGNAL DEVIATION DETECTING MEANS
CORRECTION DATA FORMING MEANS

FIG. 2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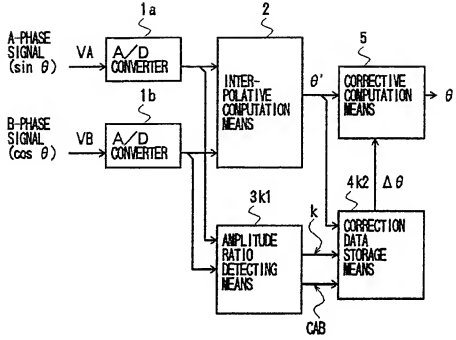
2
A-PHASE SIGNAL (sin θ)
VA
A/D CONVERTER
1b
B-PHASE SIGNAL (cos θ)
VB
A/D CONVERTER
INTER-POLATIVE COMPUTATION MEANS
θ'
5
CORRECTIVE COMPUTATION MEANS
θ
4k1
Δθ
3k
AMPLITUDE RATIO DETECTING MEANS
k
CORRECTION DATA COMPUTATION MEANS

FIG. 3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2
5
A-PHASE SIGNAL (sin θ)
VA
A/D CONVERTER
1b
B-PHASE SIGNAL (cos θ)
VB
A/D CONVERTER
INTER-POLATIVE COMPUTATION MEANS
θ'
CORRECTIVE COMPUTATION MEANS
θ
4k2
Δθ
3k1
k
CORRECTION DATA STORAGE MEANS
AMPLITUDE RATIO DETECTING MEANS
CAB

FIG. 4

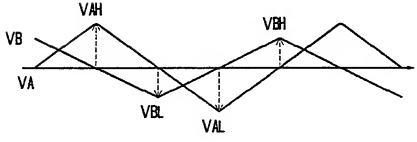

VAH
VB
VBH
VA
VBL
VAL

Fig.5

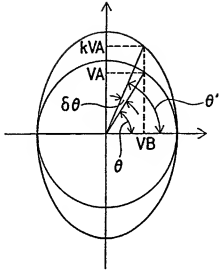


Fig.6

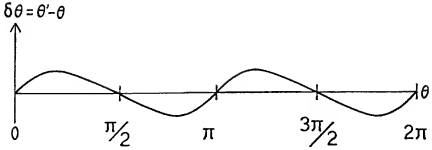


Fig.7

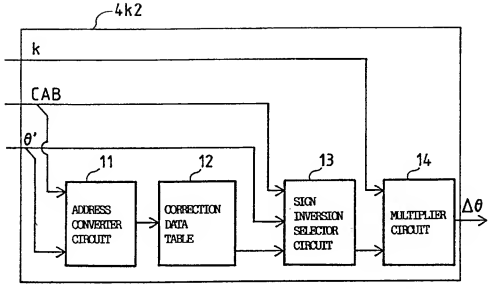

4k2
k
CAB
θ'
11
12
13
14
ADDRESS CONVERTER CIRCUIT
CORRECTION DATA TABLE
SIGN INVERSION SELECTOR CIRCUIT
MULTIPLIER CIRCUIT
Δθ

Fig.8

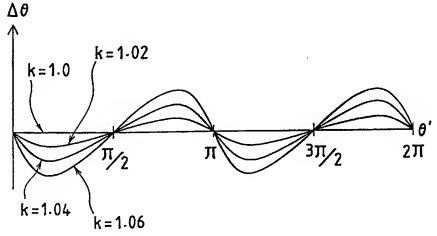

Δθ
k=1.0
k=1.02
π/2
π
3π/2
2π
θ'
k=1.04
k=1.06

FIG. 9

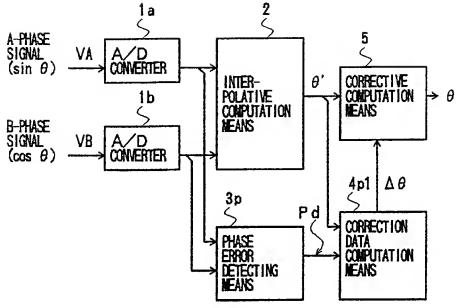

1a
2
5
A-PHASE SIGNAL (sin θ)
VA
A/D CONVERTER
INTER-POLATIVE COMPUTATION MEANS
θ'
CORRECTIVE COMPUTATION MEANS
θ
1b
B-PHASE SIGNAL (cos θ)
VB
A/D CONVERTER
4p1
Δθ
3p
Pd
PHASE ERROR DETECTING MEANS
CORRECTION DATA COMPUTATION MEANS

FIG. 10

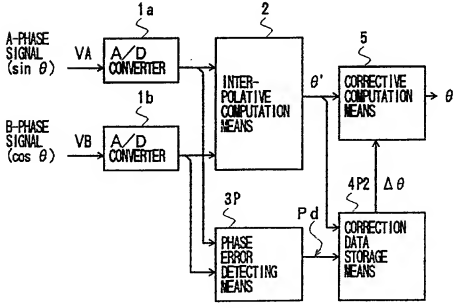

1a
2
5
A-PHASE SIGNAL (sin θ)
VA
A/D CONVERTER
INTER-POLATIVE COMPUTATION MEANS
θ'
CORRECTIVE COMPUTATION MEANS
θ
1b
B-PHASE SIGNAL (cos θ)
VB
A/D CONVERTER
4P2
Δθ
3P
Pd
PHASE ERROR DETECTING MEANS
CORRECTION DATA STORAGE MEANS

Fig. 11

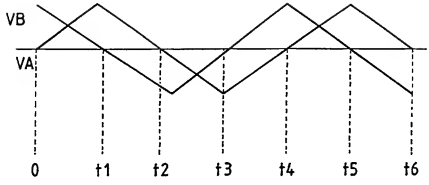


Fig. 12

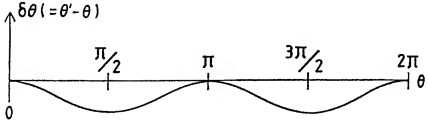


Fig.13

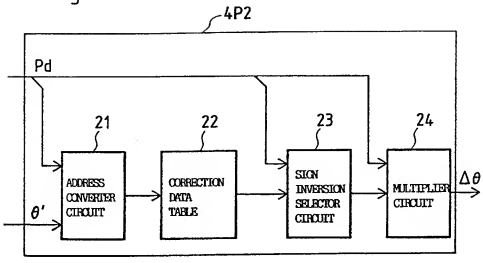

4P2
Pd
21
22
23
24
ADDRESS CONVERTER CIRCUIT
CORRECTION DATA TABLE
SIGN INVERSION SELECTOR CIRCUIT
MULTIPLIER CIRCUIT
θ'
Δθ

Fig.14

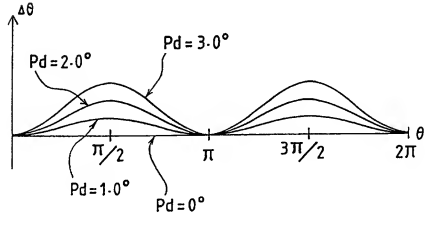
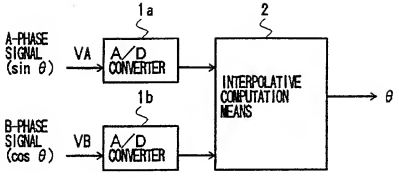

Δθ
Pd=3·0°
Pd=2·0°
π/2
π
3π/2
2π
θ
Pd=1·0°
Pd=0°

FIG. 15


1a
2
A-PHASE SIGNAL (sin θ)
VA
A/D CONVERTER
1b
B-PHASE SIGNAL (cos θ)
VB
A/D CONVERTER
INTERPOLATIVE COMPUTATION MEANS
θ

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP97/04102

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl^6 G01D5/245

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int. Cl^6 G01D5/245, G01D5/34-5/36

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho 1926 - 1996 Jitsuyo Shinan Toroku Koho 1996 - 1998
Kokai Jitsuyo Shinan Koho 1971 - 1998
Toroku Jitsuyo Shinan Koho 1994 - 1998

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP, 03-031720, A (Fanuc Ltd.), February 12, 1991 (12. 02. 91)(Family: none) Full text	1 - 4
X	JP, 07-198417, A (Siemens AG.), August 1, 1995 (01. 08. 95), Full text (Family: none)	1-4, 14-16
A		5-13, 17-19
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[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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